IN THE CLAIMS

Please cancel without prejudice, Claims 4-9 inclusively while also amending Claims 1-2 as indicated and adding new Claims 10-25 as shown in the following Claims Listing.

[Clean copies of changed specification paragraphs are provided in the Appendix]

LAW OFFICES OF
MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
(408) 392-9250
FAX (408) 392-9262

CLAIMS LISTING

1. (*Currently amended*) A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming a conductive first layer ~~comprising~~ containing primarily silicon, the first layer being to provide one or more floating gates for the nonvolatile memory;

(b) nitriding a silicon-containing surface of the first layer with a low temperature, low energy, surface nitriding process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said silicon-containing surface of the first layer at relatively low temperature and relatively low energy;

(c) subjecting the nitrided surface to a thermally oxidizing atmosphere so as to thereby form a thermally-grown ~~forming a first dielectric at the nitrided surface, wherein forming the first dielectric comprises forming~~ silicon oxide at the nitrided surface, the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms defining at least part of a first dielectric of the nonvolatile memory; and

(d) forming a conductive second layer separated ~~from the nitrided surface~~ by the first dielectric from conductive material of the first layer, the conductive second layer providing one or more control gates for the nonvolatile memory.

2. (*Currently amended*) The method of Claim 1 wherein forming the silicon oxide at the nitrided surface comprises performing oxidation at a temperature in the range 800°C-1050°C in an oxygen or oxygen/hydrogen atmosphere to thereby form ~~forming~~ the silicon oxide by thermal oxidation.

3. (*Original*) The method of Claim 1 wherein the surface of the first layer is a polysilicon surface.

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MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
(408) 392-9250
FAX (408) 392-9262

4. (*Canceled*) [[An integrated circuit manufactured by the method of claim 1.]]

5. (*Canceled*) [[An integrated circuit comprising a nonvolatile memory cell: a channel region; a first dielectric on a surface of the channel region; a conductive floating gate on the first dielectric, the floating gate having a surface which has silicon and nitrogen atoms therein; silicon oxide formed at said surface of the floating gate; a conductive control gate opposite to said surface of the floating gate.]]

6. (*Canceled*) [[The integrated circuit of claim 5 further comprising a second dielectric between said surface of the floating gate and the control gate.]]

7. (*Canceled*) [[A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising: forming a first layer to provide one or more floating gates for the nonvolatile memory; forming a first dielectric on a surface of the first layer, wherein the first dielectric comprises a first surface comprising silicon oxide; nitriding the first surface of the first dielectric to incorporate nitrogen atoms into the first surface; forming a conductive layer on the nitrided first surface of the first dielectric, the conductive layer providing one or more control gates for the nonvolatile memory.]]

8. (*Canceled*) [[An integrated circuit manufactured by the method of claim 7.]]

9. (*Canceled*) [[An integrated circuit comprising a nonvolatile memory cell comprising: a channel region; a first dielectric on a surface of the channel region; a conductive floating gate on the first dielectric; a second dielectric on a surface of the floating gate; and a conductive control gate separated from the floating gate by the second dielectric; wherein the second dielectric comprises a layer of silicon oxide having a surface having

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MacPherson Kwok Chen & Heid
LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
(408) 392-9250
FAX (408) 392-9262

nitrogen atoms embedded therein; and the control gate contacts said silicon oxide surface with nitrogen atoms.]]

10. (New) The method of Claim 1 wherein the nitriding step includes using a Remote Plasma Nitridation (RPN) process.

11. (New) The method of Claim 1 wherein the nitriding step includes using a Decoupled Plasma Nitridation (DPN) process.

12. (New) The method of Claim 1 wherein the nitriding step provides a concentration of nitrogen atoms of 1-20 atomic percent in the nitrided surface.

13. (New) The method of Claim 12 wherein the nitriding step incorporates said nitrogen atoms to a depth of no more than 3 nm in said surface of the first layer.

14. (New) The method of Claim 1 wherein said first layer is disposed over a tunneling dielectric.

15. (New) The method of Claim 14 and further comprising: thermally growing the tunneling dielectric.

16. (New) The method of Claim 1 and further comprising: depositing a silicon nitride layer on said combination of the thermally-grown silicon oxide and incorporated nitrogen atoms to thereby define a further part of the first dielectric of the nonvolatile memory.

17. (New) The method of Claim 16 and further comprising: depositing a silicon oxide layer on said deposited silicon nitride layer to thereby define a yet further part of the first dielectric of the nonvolatile memory.

18. (New) A method of manufacturing a nonvolatile memory cell within a monolithically integrated circuit, the method comprising:

(a) forming a tunneling dielectric layer on a semiconductive substrate;

(b) forming a floating gate layer on said tunneling dielectric layer, the floating gate layer having a top surface composed primarily of conductive silicon;

(c) surface nitridating said top surface of the floating gate layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled

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MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
(408) 392-9250
FAX (408) 392-9262

Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said top surface of the floating gate layer at relatively low temperature and relatively low energy; and

(d) subjecting the nitrided top surface to a thermally oxidizing atmosphere so as to thereby form a combination of thermally-grown silicon oxide and surface incorporated and thermally treated nitrogen atoms at the nitrided and thermally oxidized top surface of the floating gate layer.

19. (New) The memory cell manufacturing method of Claim 18 and further comprising:

(e) depositing a silicon nitride layer directly on the nitrided and thermally oxidized top surface of the floating gate layer.

20. (New) The memory cell manufacturing method of Claim 19 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

21. (New) The memory cell manufacturing method of Claim 19 and further comprising:

(f) depositing a silicon oxide layer directly on the silicon nitride layer.

22. (New) The memory cell manufacturing method of Claim 21 and further comprising:

(g) surface nitridating said deposited silicon oxide layer with a low temperature, low energy process such as Remote Plasma Nitridation (RPN) or Decoupled Plasma Nitridation (DPN) so as to incorporate nitrogen atoms into said deposited silicon oxide layer at relatively low temperature and relatively low energy.

23. (New) The memory cell manufacturing method of Claim 22 and further comprising:

(h) forming a conductive gate layer on said surface nitridated and deposited silicon oxide layer.

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San Jose, CA 95110
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FAX (408) 392-9262

24. (New) The memory cell manufacturing method of Claim 18 and further wherein:

(d.1) said subjecting of the nitrided top surface to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface to form thermally grown silicon dioxide at the top of the nitrided and thermally oxidized top surface.

25. (New) The memory cell manufacturing method of Claim 18 and further wherein:

said surface nitridating step incorporates nitrogen atoms into the said top surface of the floating gate layer to a depth of less than 3nm.

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FAX (408) 392-9262